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What is claimed is:

CLAIMS

a later time;

| 1 | 1. A method for accessing a computer memory array, the method comprising | |
|----------------|---|--|
| 2 | receiving a set of initial address bits from a memory manager, said initial | |
| 3 | address bits corresponding to a memory location defined in a first format; and | |
| 4 | translating said set of initial address bits to a set of translated address bits | |
| 5 | said translated address bits corresponding to a memory location defined in a second | |
| 6 | format. | |
| 10 20 20 | 2. The method of claim 1, further comprising: receiving a set of row address bits from said memory manager at a first | |

time; receiving a set of initial column address bits from said memory manager at

translating said set of initial column address bits to a set of translated column address bits; and

simultaneously using said set of row address bits and said set of translated column address bits to access a desired memory location in the memory array;

wherein said desired memory location in the memory array has a row address corresponding to the value of said set of row address bits and a column address corresponding to the value of said set of translated column address bits.

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| 1 | 3. | The method of claim 2, wherein: | |
|----------------------------|--|---|--|
| 2 | | a first subset of said initial address bits is used to generate said translated | |
| 3 | column address bits; and | | |
| 4 | | a second subset of initial address bits is used to identify a specific location | |
| 5 | within a men | nory array column corresponding to said translated column address bits. | |
| 1 | 4. | The method of claim 3, wherein: | |
| 2 | | said memory manager processes memory address information in | |
| 3 | accordance with a first memory page structure; and | | |
| 4 | | the memory array is configured in accordance with a second memory page | |
| 5□ | structure; | | |
| ·⊔ 6: <u>□</u> | | wherein a memory page structure is defined by the number of columns | |
| 7 . = | included in a given row, and the number of storage locations located at each column in | | |
| 59997 79997 8599 | w. | | |
| 1= | 5. | The method of claim 4, wherein: | |
| 2,5 | | said first memory page structure and said second memory page structure | |
| 3H | contain an unequal number of columns; and | | |
| 15 27 35 35 44 | | said first and second memory page structures contain an equal number of | |
| 5 | storage locat | ions. | |
| | | | |

| 1 | 6. A method for decoding a memory array address for an embedded DRAM | |
|---------------------------|---|--|
| 2 | (eDRAM) device, the eDRAM device configured for operation with an SDRAM memory | |
| 3 | manager, the method comprising: | |
| 4 | receiving a set of row address bits from the memory manager at a first | |
| 5 | time; | |
| 6 | receiving a set of initial column address bits from the memory manager at | |
| 7 | a later time; | |
| 8 | translating said set of initial column address bits to a set of translated | |
| 9 | column address bits; and | |
| 10 | simultaneously using said set of row address bits and said set of translated | |
| 11 | column address bits to access a desired memory location in the eDRAM device; | |
| 11 0 120 120 | wherein said desired memory location in the eDRAM device has a row | |
| 13 <mark>5</mark> | address corresponding to the value of said set of row address bits and a column address | |
| 142 | corresponding to the value of said set of translated column address bits. | |
| | | |
| 1 | 7. The method of claim 6, wherein: | |
| 2 1 | a first subset of said initial address bits is used to generate said translated | |
| 311 | column address bits; and | |
| | a second subset of initial address bits is used to identify a specific location | |
| 5 | within an eDRAM column corresponding to said translated column address bits. | |

| 1 | 8. The method of claim 7, wherein: | | |
|--|--|--|--|
| 2 | the SDRAM memory manager processes memory address information in | | |
| 3 | accordance with a first memory page structure; and | | |
| 4 | the eDRAM device is configured in accordance with a second memory | | |
| 5 | page structure; | | |
| 6 | wherein a memory page structure is defined by the number of columns | | |
| 7 | included in a given row, and the number of storage locations located at each column in | | |
| 8 | said given row. | | |
| | | | |
| 1 | 9. The method of claim 8, wherein: | | |
| 2 🚍 | said first memory page structure and said second memory page structure | | |
| 3 <u>:</u> | contain an unequal number of columns; and | | |
| 4 | said first and second memory page structures contain an equal number of | | |
| 20 30 40 50 10 20 30 40 30 40 40 40 40 40 40 40 40 40 40 40 40 40 | storage locations. | | |
| of the same | | | |
| 1 3 | 10. An apparatus for decoding a memory array address for an embedded | | |
| 2 ^M | DRAM (eDRAM) device, the eDRAM device configured for operation with an SDRAM | | |
| 3 <u>D</u> | memory manager, the apparatus comprising: | | |
| 4 | a register for receiving a set of row address bits from the memory manager | | |
| 5 | at a first time; | | |
| 6 | a counter for receiving a set of initial column address bits from the | | |
| 7 | memory manager at a later time; and | | |
| 8 | a broadside address register for simultaneously receiving a first subset of | | |
| 9 | said set of initial column address bits and said row address bits; | | |
| 10 | wherein said first subset of said set of initial column address bits defines a | | |
| 11 | translated column address for the eDRAM device. | | |

| 1 | 11. The apparatus of claim 10, further comprising. | | |
|-------|--|--|--|
| 2 | a multiplexing device for receiving a second subset of said set of initial | | |
| 3 | column address bits; | | |
| 4 | wherein said second subset of said set of initial column address bits | | |
| 5 | corresponds to a specific storage location segment within said translated column address | | |
| 1 | 12. The apparatus of claim 11, wherein the eDRAM device includes a first | | |
| 2 | eDRAM module coupled with a second eDRAM module. | | |
| 1 | 13. The apparatus of claim 12, further comprising: | | |
| 2 💆 | steering logic for determining in which of said first and second eDRAM | | |
| | modules said specific storage location segment is contained. | | |
| 111 | 14. The apparatus of claim 13, wherein an input to said steering logic | | |
| 2[] | comprises a third subset of said set of initial column address bits. | | |
| | 15. A computer memory system, comprising: | | |
| 2.0 | an SDRAM memory controller; | | |
| 3 = 1 | an embedded DRAM (eDRAM) device integrated with said SDRAM | | |
| 4 | memory controller; and | | |
| 5 | an address decoding apparatus for translating a memory address generate | | |
| 6 | by said SDRAM memory controller to a translated memory address in said eDRAM | | |
| 7 | device. | | |
| | | | |

| 1 | 16. | The computer memory system of claim 15, wherein said address decoding | |
|--|--|---|--|
| 2 | apparatus further comprises: | | |
| 3 | | a register for receiving a set of row address bits from the memory | |
| 4 | controller at a first time; | | |
| 5 | | a counter for receiving a set of initial column address bits from the | |
| 6 | memory controller at a later time; and | | |
| 7 | | a broadside address register for simultaneously receiving a first subset of | |
| 8 | said set of initial column address bits and said row address bits; | | |
| 9 | | wherein said first subset of said set of initial column address bits defines a | |
| 10 | translated column address for the eDRAM device. | | |
| 10 10 10 10 10 10 10 10 10 10 10 | 18. | The computer memory system of claim 16, further comprising: a multiplexing device for receiving a second subset of said set of initial ess bits; wherein said second subset of said set of initial column address bits to a specific storage location segment within said translated column address. The computer memory system of claim 17, wherein the eDRAM device est eDRAM module coupled with a second eDRAM module. | |
| 1 2 | 19. | The computer memory system of claim 18, further comprising: steering logic for determining in which of said first and second eDRAM | |
| 3 | modules said | I specific storage location segment is contained. | |
| 1 | 20. | The computer memory system of claim 19, wherein an input to said | |

steering logic comprises a third subset of said set of initial column address bits.

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21. A method of translating initial column storage locations defined in a first memory array structure to corresponding storage locations in a second memory array structure, the first memory array structure having X columns associated therewith and capable of storing an M-bit data word at each memory address therein, the second memory array structure having Y columns associated therewith and capable of storing an N-bit data word at each memory address therein, wherein XM = YN, X > Y, and M < N, the method comprising:

dividing the N-bit data word in each column associated with the second memory array structure into N/M word slices, each of said word slices serving as an M-bit storage location; and

assigning each initial column storage location to one of said word slices.